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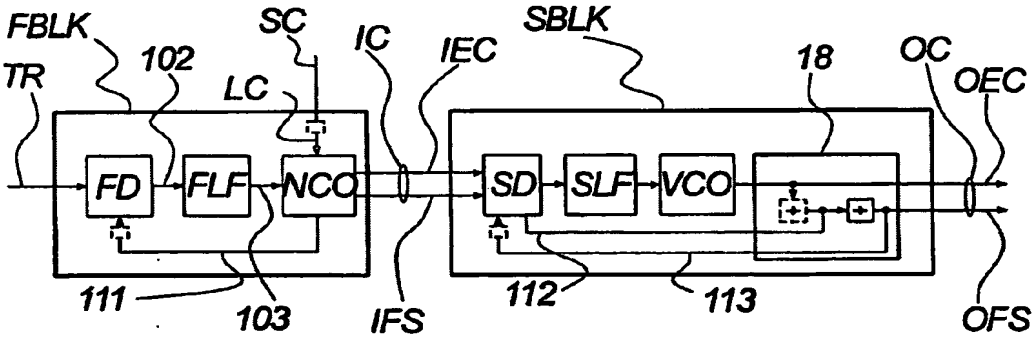
(54) Title: METHOD OF ESTABLISHING AN OSCILLATOR CLOCK SIGNAL



(57) Abstract: A hybrid numeric-analog clock synchronizer, for establishing a clock or carrier locked to a timing reference. The clock may include a framing component. The reference may have a low update rate. The synchronizer achieves high jitter rejection, low phase noise and wide frequency range. It can be integrated on chip. It may comprise a numeric time-locked loop (TLL) with an analog phase-locked loop (PLL). Moreover a high-performance number-controlled oscillator (NCO), for creating an event clock from a master clock according to a period control signal. It processes edge times rather than period values, allowing direct control of the spectrum and peak amplitude of the justification jitter. Moreover a combined clock-and-frame asynchrony detector, for measuring the phase or time offset between composite signals. It responds e.g. to event clocks and frame syncs, enabling frame locking with loop bandwidths greater than the frame rate.

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